

DATA SHEET

NE1619

HECETA 4

Temperature and voltage monitor

Product data
Supersedes data of 2000 Jul 13

2001 Aug 29

HECETA4 Temperature and voltage monitor

NE1619

GENERAL DESCRIPTION

The NE1619 is designed for monitoring the temperatures and supply voltages of microprocessor-based systems by measuring those parameters and comparing the readings with programmable limits. The device provides five possible analog inputs, a remote temperature sensor input and on-board local temperature sensor. The device also monitors its own power supply and provides digital inputs for the Pentium/PRO power supply ID code.

The device communicates with the system controller via an SMBus (System Management bus) by which it can be programmed for operation and data collection. Readings come from conversions of the on-board A-to-D converter which cycles through all measurements in sequence in approximately one second when the conversion is started. The device includes a number of registers to store data of the device configuration, status, readings and limits. Except for the temperature-related data which are in 8-bit digital 2's complement format, all the data are in 8-bit digital straight format.

FEATURES

- Monitor local and remote temperatures
- Temperature accuracy of ± 2 °C for local, and ± 3 °C for remote channel
- Temperature resolution of 1 °C
- 2.8 V to 5.5 V supply range

- Monitor different power supplies: 12 V, 5 V, 3.3 V, 2.5 V, V_{CCP} , V_{DD}
- V_{IN} accuracy of $\pm 2\%$ of full scale
- Differential non-linearity of ± 1 LSB
- No calibration required
- Programmable temperature and voltage limits for alarms
- Programmable Reset low state pulse output
- SMBus 2-wire serial interface
- Small 16-lead SSOP package
- Compatible with Intel "Heceta 4" specification and reference designs utilizing it

APPLICATIONS

- System thermal and hardware monitor
- Desktop computers
- Notebook computers
- Industrial controllers
- Telecom equipment

ORDERING INFORMATION

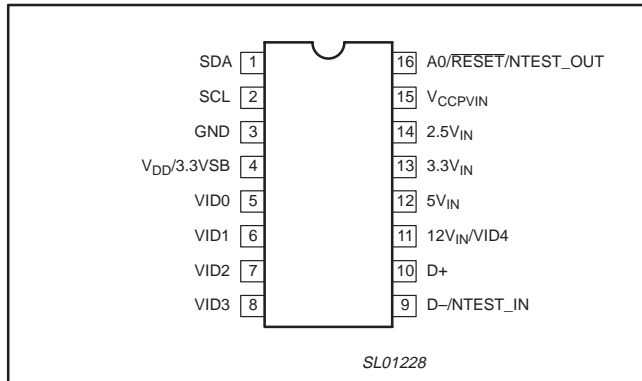
PART NUMBER	PACKAGE	DRAWING NUMBER
NE1619DS	SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT519-1

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PINNING

Pin Configuration



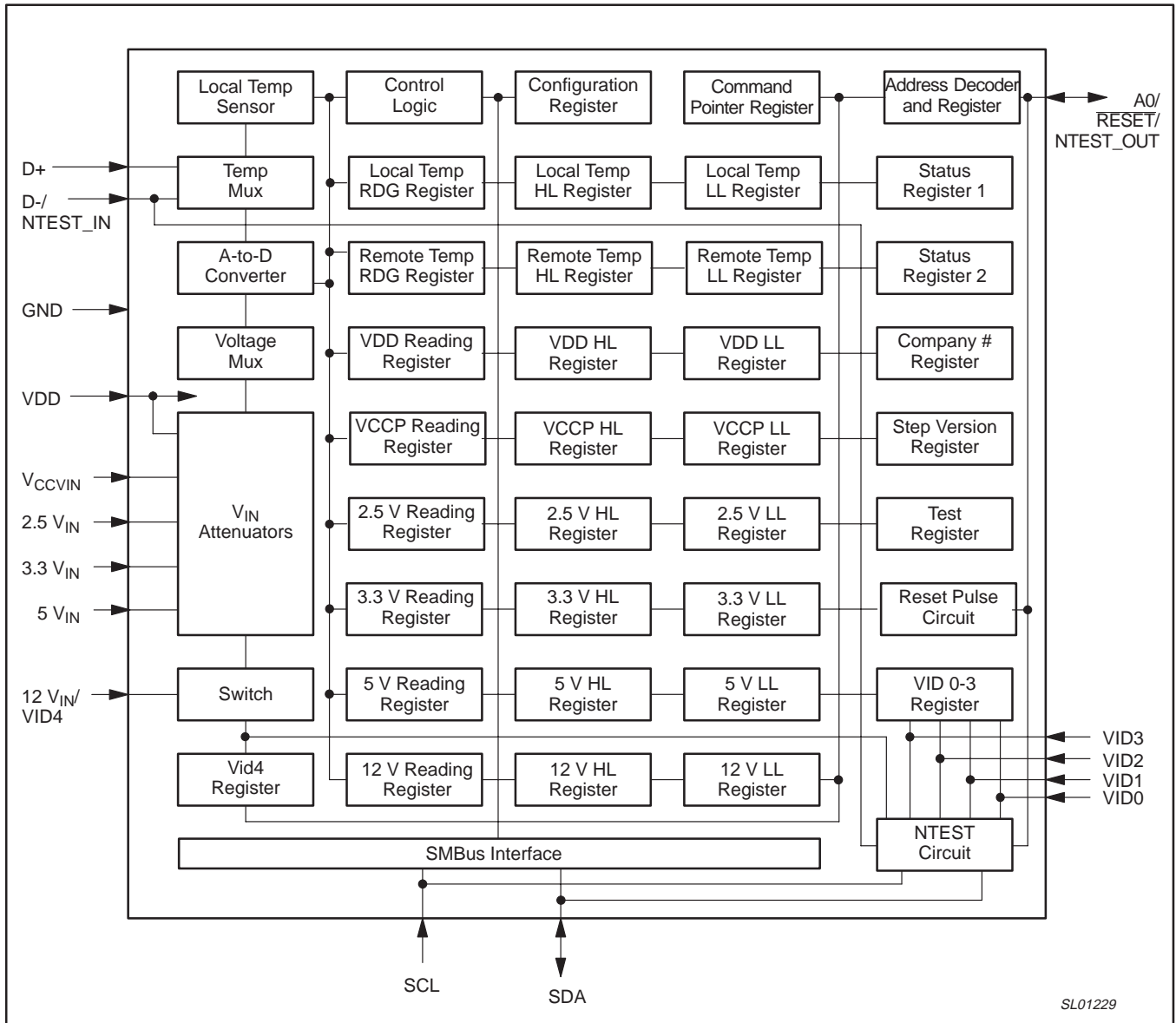
Pin Description

PIN #	SYMBOL	FUNCTION DESCRIPTION
1	SDA	Digital I/O. SMBus serial bi-directional data. Open-drain output.
2	SCL	Digital Input. SMBus serial clock input.
3	GND	Ground. To be connected to system ground.
4	V _{DD} /3.3VSB	Power supply. Can be connected to +3.3 V standby power if monitoring in low power states is required. This pin also serves as the analog input to monitor the V _{DD} voltage level.
5	VID0	Digital Input. For Voltage ID readouts from the processor. This value is read into the VID status register (LSB bit).
6	VID1	Digital Input. For Voltage ID readouts from the processor. This value is read into the VID status register.
7	VID2	Digital Input. For Voltage ID readouts from the processor. This value is read into the VID status register.
8	VID3	Digital Input. For Voltage ID readouts from the processor. This value is read into the VID status register.
9	D-/NTEST_IN	Analog/Digital Input. This pin is connected to the negative terminal of the remote temperature sensor for analog input. If this pin is held high at power-up, for digital input, it enables the NAND-TREE test mode.
10	D+	Analog Input. This pin is connected to the positive terminal of the remote temperature sensor.
11	12V _{IN} /VID4	Analog/Digital Input. Defaults at power-up to analog input for monitoring the +12 V supply. This pin is programmable to be a digital input for voltage ID readouts from the processor. Its state is read into the VID4 status register.
12	5V _{IN}	Analog Input. For monitoring the +5 V supply.
13	3.3V _{IN}	Analog Input. For monitoring the +3.3 V supply.
14	2.5V _{IN}	Analog Input. For monitoring the +2.5 V supply.
15	V _{CCPVIN}	Analog Input. For monitoring the processor voltage supply (0 to 3.0 V)
16	A0/RESET/NTEST_IN	Digital I/O. At power-up, the logic input of this pin defines the LSB bit of the device slave address. This pin can be configured to give a low pulse reset output of 20ms minimum. This pin also functions as the output in the NAND-TREE test mode.

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FUNCTIONAL BLOCK DIAGRAM

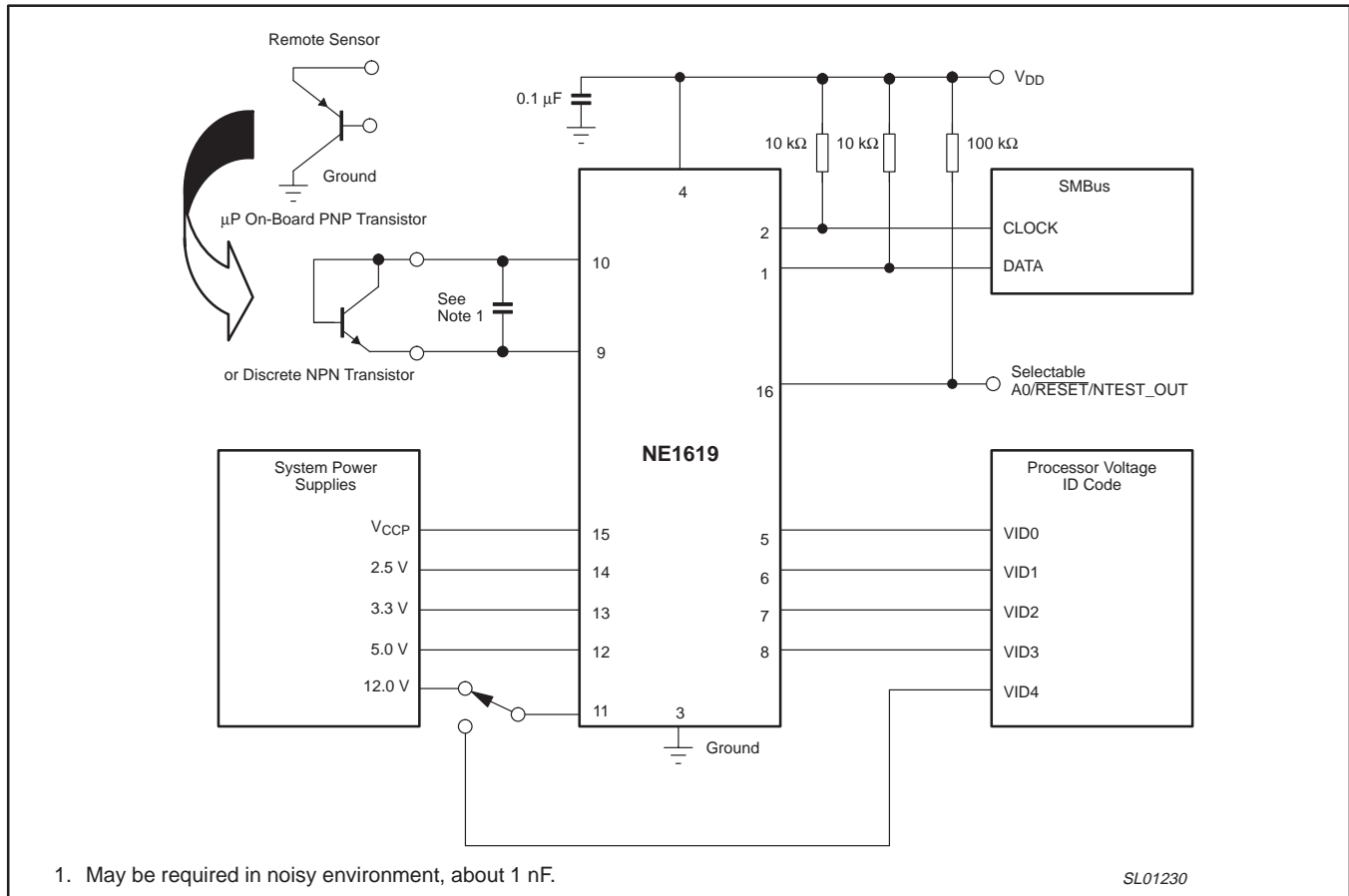


SL01229

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TYPICAL OPERATING CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN.	MAX.	UNIT
V _{DD} to GND	-0.3	6	V
12V _{IN} to GND	-0.3	18	V
5V _{IN} , 3.3V _{IN} , 2.5V _{IN} , V _{CCP} to GND	-0.3	6	V
Other pins to GND	-0.3	V _{DD} +0.3	V
Input current at any pin	-5	5	mA
Package input current	-20	20	mA
Operating temperature range	0	+120	°C
Maximum junction temperature		+150	°C
Storage temperature range	-65	+150	°C

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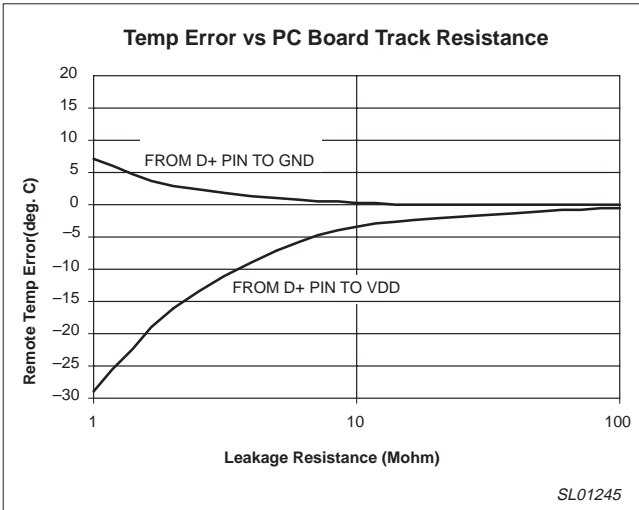


Figure 1. Temp Error versus PC Board Track Resistance

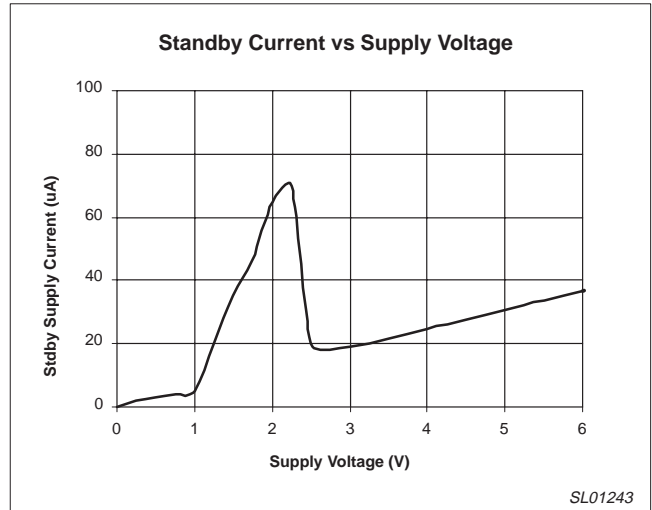


Figure 3. Standby Current versus Supply Voltage

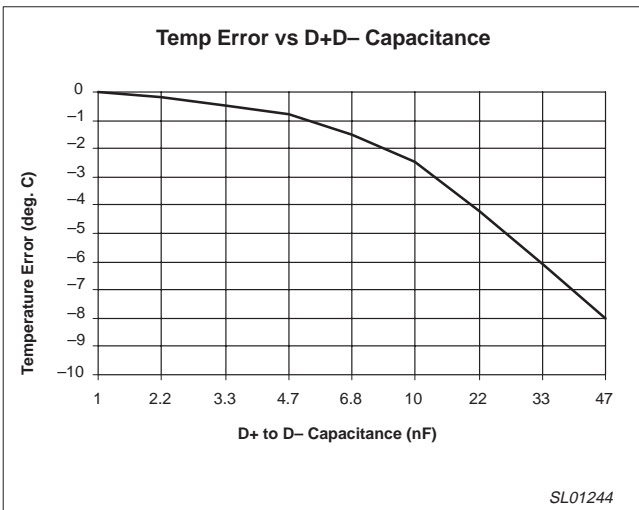


Figure 2. Temp Error versus D+D- Capacitance

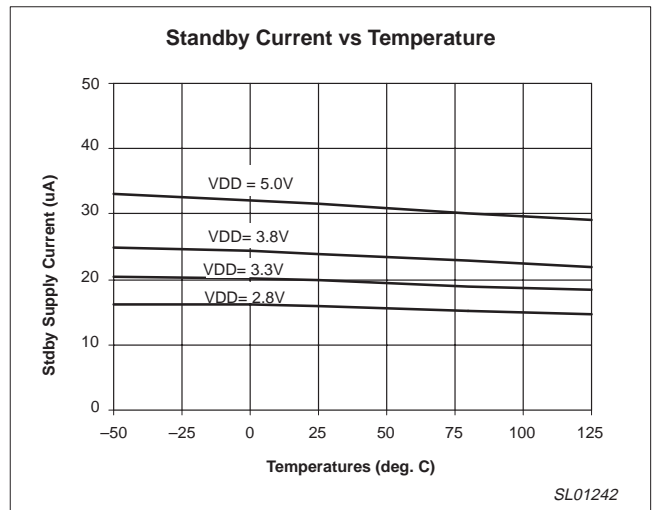


Figure 4. Standby Current versus Temperature

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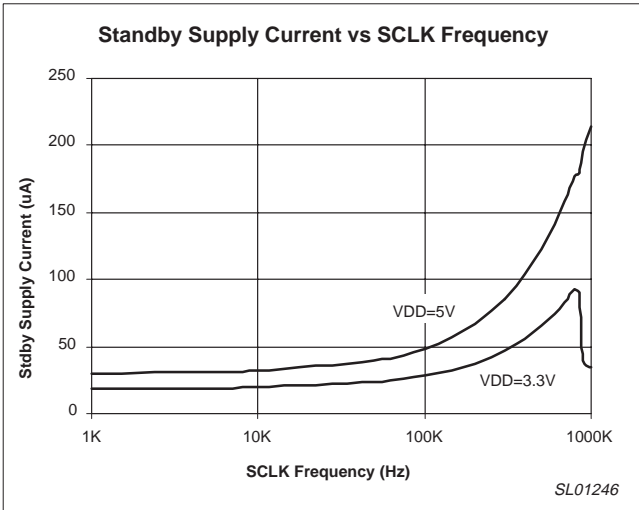


Figure 5. Standby Current versus SCLK Frequency

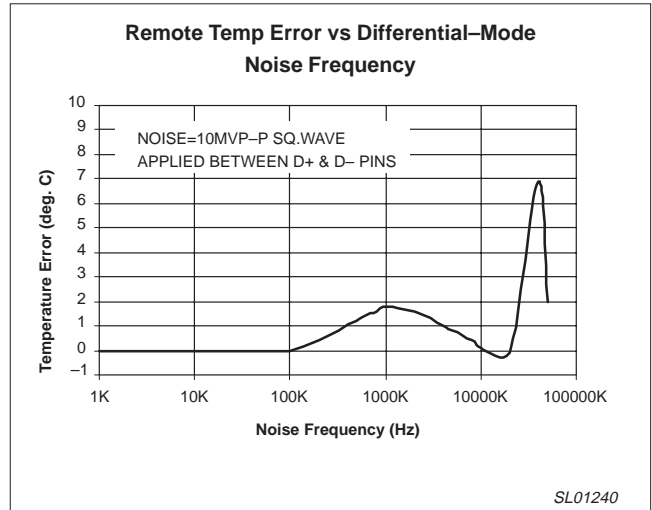


Figure 7. Temp error versus Different Mode Noise Frequency

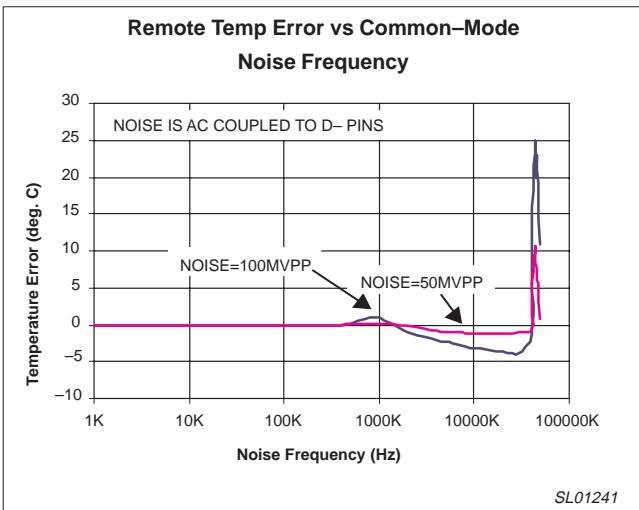


Figure 6. Temp Error versus Common Mode Noise

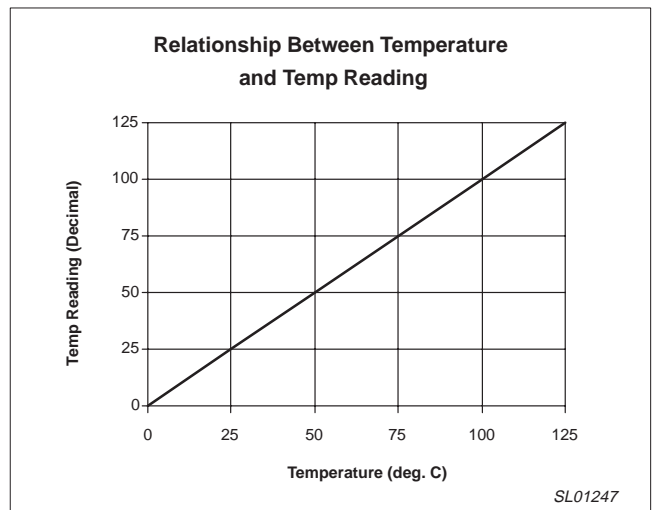


Figure 8.

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DC ELECTRICAL CHARACTERISTICS $V_{DD} = 3.3\text{ V}$, $T_{amb} = 0\text{ °C}$ to $+120\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage		2.8	3.3	5.5	V
I_{DD}	Supply current	Standby mode		100		μA
I_{DD}	Supply current	Operating mode		250	500	μA
t_C	Total monitoring cycle time ¹	All conversions		0.25	0.50	sec
T_R	Temperature resolution	Local and Remote		± 1.0		$^{\circ}\text{C}$
T_{AI}	Internal temperature accuracy	$T_{amb} = 25\text{ °C}$			± 2.0	$^{\circ}\text{C}$
		$T_{amb} = 0\text{ °C}$ to $+120\text{ °C}$			± 3.0	$^{\circ}\text{C}$
T_{AE}	External temperature accuracy	$T_{amb} = 25\text{ °C}$			± 3.0	$^{\circ}\text{C}$
		$T_{amb} = 0\text{ °C}$ to $+120\text{ °C}$			± 5.0	$^{\circ}\text{C}$
I_S	Remote source current	High level		100		μA
		Low level		10		μA
Voltage-to-Digital converter ($12V_{IN}$, $5V_{IN}$, $3.3V_{IN}$, $2.5V_{IN}$, V_{CCP}, V_{DD})						
VUE	Unadjusted error				± 2.0	%FS
VDNL	Differential non-linearity error			± 1.0		LSB
VRIN	V_{IN} input resistance		100	200		$\text{k}\Omega$
VPSS	V_{IN} power supply sensitivity			± 1.0		%/V
Digital output (SDA, A0²)						
V_{OH}	Output High voltage	$I_{OUT} = -3.0\text{ mA}$, $V_{DD} = 2.8\text{ V}$			2.4	V
V_{OL}	Output Low voltage	$I_{OUT} = 3.0\text{ mA}$, $V_{DD} = 3.8\text{ V}$	0.4			V
I_{OH}	Output High leakage current	$V_{OUT} = V_{DD}$		0.1	10.0	μA
SMB digital input voltages (SDA, SCL)						
V_{IH}	Input High voltage				$0.6V_{DD}$	V
V_{IL}	Input Low voltage				$0.3V_{DD}$	V
Digital input voltages (A0, VID0–4, NT_IN³)						
V_{IH}	Input High voltage				2.0	V
V_{IL}	Input Low voltage		0.4			V
Digital input current (all digital inputs)						
I_{IH}	Input High current	$V_{IN} = V_{DD}$	-1.0			μA
I_{IL}	Input Low current	$V_{IN} = \text{GND}$			1.0	μA
C_{IN}	Input capacitance			20.0		pF

NOTES:

- Total monitoring cycle time includes all temperature conversions and all voltage conversions.
- When A0 is selected as output in NAND-TREE test mode.
- When D- is selected as input in NAND-TREE test mode.

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SMBus INTERFACE AC CHARACTERISTICS

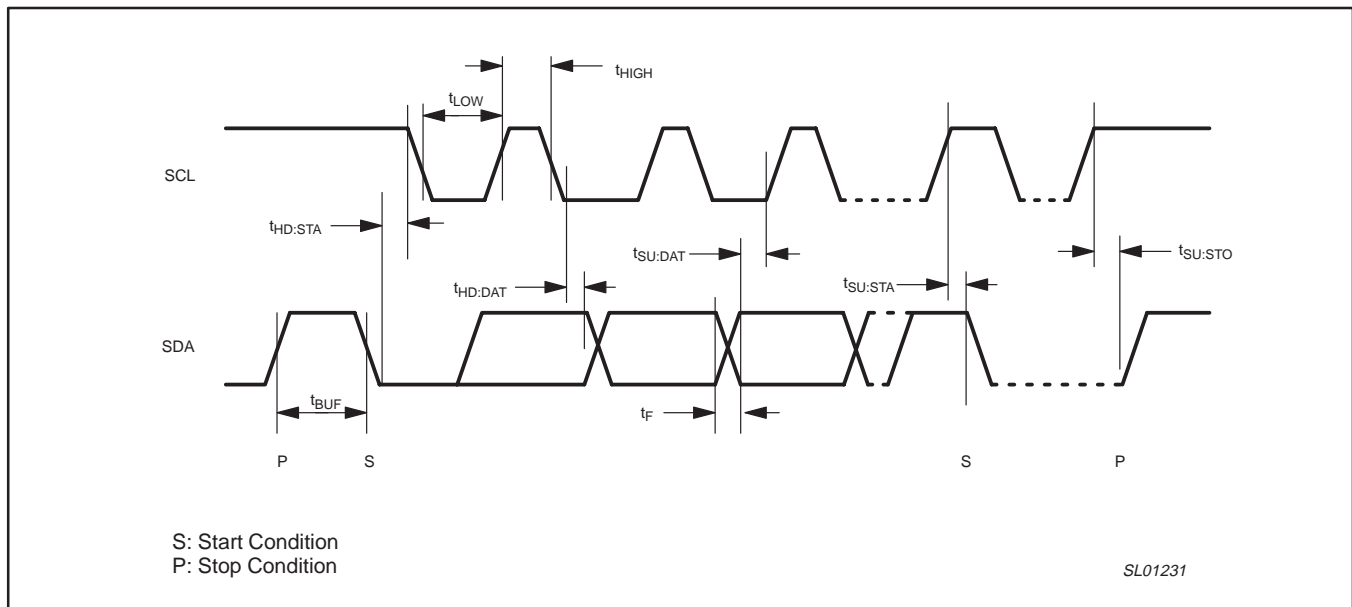
$V_{DD} = 3.3\text{ V}$, $T_{amb} = 0\text{ }^{\circ}\text{C}$ to $+120\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{SCL}	SCL clock frequency				400	kHz
t_{BUF}	SMBus free time		4.7			μs
t_{LOW}	SCL Low time		4.7			μs
t_{HIGH}	SCL High time		4.0			μs
$t_{SU:STA}$	Start set-up time		100			ns
$t_{HD:STA}$	Start hold time		100			ns
$t_{SU:STO}$	Stop set-up time		4.0			μs
$t_{SU:DAT}$	Data set-up time		250			ns
$t_{HD:DAT}$	Data hold time		0			ns
t_F	Fall time				1.0	μs

NOTE:

1. These specifications are guaranteed by design and not tested in production.

TIMING DIAGRAM



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Table 1. List of registers

NAME	COMMAND OR ADDRESS	R/W	POR STATE	DESCRIPTION
CR	40h	R/W	0000 1000	Configuration register
SR1	41h	Read only	0000 0000	Status register #1
SR2	42h	Read only	0000 0000	Status register #2
VID	47h	Read only	0000 xxxx	VID register, xxxx = VID3–VID0
VID4	49h	Read only	1000 000x	VID4 register, x = VID4
CID	3Eh	Read only	1010 0001	Company number
SID	3Fh	Read only	0010 0001	Stepping version number
TEST	15h	R/W	N/A	Manufacturer test register
2.5VR	20h	Read only	N/A	2.5V _{IN} reading register
VCCPR	21h	Read only	N/A	V _{CCPVIN} reading register
3.3VR	22h	Read only	N/A	3.3V _{IN} reading register
5VR	23h	Read only	N/A	5V _{IN} reading register
12VR	24h	Read only	N/A	12V _{IN} reading register
VDDR	25h	Read only	N/A	V _{DD} reading register
ETR	26h	Read only	N/A	External or remote temperature reading register
ITR	27h	Read only	N/A	Internal or local temperature reading register
2.5VHL	2Bh	R/W	0000 0000	2.5V _{IN} high limit register
2.5VLL	2Ch	R/W	0000 0000	2.5V _{IN} low limit register
VCCPHL	2Dh	R/W	0000 0000	V _{CCPVIN} high limit register
VCCPLL	2Eh	R/W	0000 0000	V _{CCPVIN} low limit register
3.3VHL	2Fh	R/W	0000 0000	3.3V _{IN} high limit register
3.3VLL	30h	R/W	0000 0000	3.3V _{IN} low limit register
5VHL	31h	R/W	0000 0000	5V _{IN} high limit register
5VLL	32h	R/W	0000 0000	5V _{IN} low limit register
12VHL	33h	R/W	0000 0000	12V _{IN} high limit register
12VLL	34h	R/W	0000 0000	12V _{IN} low limit register
VDDHL	35h	R/W	0000 0000	V _{DDVIN} high limit register
VDDL	36h	R/W	0000 0000	V _{DDVIN} low limit register
ETHL	37h	R/W	0000 0000	External or remote temperature high limit register
ETLL	38h	R/W	0000 0000	External or remote temperature low limit register
ITHL	39h	R/W	0000 0000	Internal or local temperature high limit register
ITLL	3Ah	R/W	0000 0000	Internal or local temperature low limit register

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Table 2. Configuration Register (CR, 40h, default = 0000 1000)

BIT	NAME	R/W	DESCRIPTION
0	START	R/W	Logic 1 enables startup of monitor device, logic 0 places the device in standby mode. Power-up default = 0. At startup, limit checking functions and scanning begins. Note, all High and Low limits should be set into the ASIC prior turning on this bit.
1	Reserved	Read	Power-up default = 0.
2	Reserved	Read	Power-up default = 0.
3	Reserved	Read	Power-up default = 1.
4	RESET	R/W	Setting this bit generates a minimum 20ms low pulse on the Reset pin, if the reset function is enabled. Power-up default = 0.
5	12V _{IN} /VID4 SELECT	R/W	Selects whether pin 11 acts as a 12 volt analog input monitoring pin, or as a VID[4] input. This pin defaults to the 12 volt analog input. Power-up default = 0.
6	Reserved	Read	Power-up default = 0.
7	Initialization	R/W	Logic 1 restores power-up default values to the configuration register and the status registers. This bit automatically clears itself. Power-up default = 0.

Table 3. Status Register 1 (SR1, 41h, default = 0000 0000)

BIT	NAME	R/W	DESCRIPTION
0	+2.5V_ERROR	Read	A one indicates 2.5V _{IN} High or Low limit has been exceeded.
1	VCCP_ERROR	Read	A one indicates V _{CCPVIN} High or Low limit has been exceeded.
2	+3.3V_ERROR	Read	A one indicates 3.3V _{IN} High or Low limit has been exceeded.
3	+5V_ERROR	Read	A one indicates 5V _{IN} High or Low limit has been exceeded.
4	Internal Temp Error	Read	A one indicates internal or local temp High or Low limit has been exceeded.
5	External Temp Error	Read	A one indicates external or remote temp High or Low limit has been exceeded.
6	Reserved	Read	
7	Reserved	Read	

Table 4. Status Register 2 (SR2, 42h, default = 0000 0000)

BIT	NAME	R/W	DESCRIPTION
0	+12V_ERROR	Read	A one indicates 12V _{IN} High or Low limit has been exceeded.
1	VDD_ERROR	Read	A one indicates V _{DD} High or Low limit has been exceeded.
2	Reserved	Read	Undefined.
3	Reserved	Read	Undefined.
4	Reserved	Read	Undefined.
5	Reserved	Read	Undefined.
6	Remote Diode Fault	Read	A one indicates either a short or open circuited fault on the remote thermal diode inputs.
7	Reserved	Read	Undefined.

Table 5. VID (VID, 47h, default = 0000 VID[3:0])

BIT	NAME	R/W	DESCRIPTION
0–3	VID[0:3]	Read	The VID[0:3] inputs from Pentium/PRO power supplies ID to indicate the operating voltage (e.g. 1.5V to 2.9V). Power-up default = VID[0:3].
4–6	Reserved	Read	Undefined.
7	RESET ENABLE	Read	When set to 1, enables the RESET pin output function. This bit defaults to 0 at Power-up and enables addressing function.

Table 6. VID4 (VID4, 49h, default = 1000 000VID[4])

BIT	NAME	R/W	DESCRIPTION
0	VID4	Read	VID4 input, if selected, from Pentium/PRO power supplied ID. Power-up default = 0 and pin 11 is not selected for VID4.
1–7	Reserved	Read	Power-up default = 1000 000

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FUNCTIONAL DESCRIPTION

SMBus serial interface

The NE1619 can be connected to a compatible 2-wire serial interface SMBus as a slave device under the control of a master device or controller, using two device terminals SCL and SDA. The controller will provide a clock signal to the device SCL pin and write/read data to/from the device through the SDA pin.

Data of 8-bit digital byte or word are used for communication between the controller and the device.

Notice that external pull-up resistors, about 10 kΩ, are needed for the two terminals SCL and SDA.

Slave address

The NE1619 slave address on the SMBus is defined by the hardware connection applied to the device pin 16. At power-up this pin is automatically reset to its address sensing function A0. This logic input will set up the value of the LSB bit of the 7-bit address. Because A0 is a two-level digital input and the other 6 bits of the address are predefined to 010110, only two slave addresses can be used as listed below for the device:

Table 7.

A0 connection (Pin 16)	Slave address
GND	0101100
V _{DD}	0101101

Because the logic is sampled and latched into the device storage only at power-up, the device pin 16 can be programmed for different functions while power is on without effecting the address definition.

Registers

The NE1619 contains a number of registers, as listed in Table 1, in order to store data of the device setup and operation results. The table indicates the command value and read/write capability of each register for SMBus communication and also the power-up default values for some registers. It includes:

- Configuration register to provide control and configuration as well as initialization the NE1619,
- Status registers to provide the flags resulting from limit comparisons,
- Reading registers to store results of measurements,
- Limit registers to store programmable limit data,
- ID and test registers.

Data are stored in registers by 8-bit digital byte, either in 2's complement format for temperature-related data or in straight format for others. Writing and reading registers will be done on the SMBus by a controller using the SMBus protocols that will be described more in the last section of this functional description. Notice that attempting to write to a "Read only" register will produce an invalid result.

Power-on reset

When the power is applied to the NE1619, also called hardware reset, the registers are reset to their default value, if defined, as shown in Table 1. The content of registers which have indeterminate default value such as reading registers will be unknown. The on-board A-to-D converter is disabled and the monitoring function is not started. The device enters standby mode and draws a supply current less than 100 μA.

Because all limit registers are reset to zero, writing limits into the limits registers should usually be the first action to be performed after power-on reset.

Initialization

Initialization or software reset of the NE1619 can be initiated by setting bit 7 of the configuration register. This bit automatically clears itself after being set. The initialization performs a similar reset function to power-on reset, except that the reading and limit registers are not reset.

Starting conversion

The NE1619 monitoring function is started by setting (to 1) the START bit (bit 0) of the configuration register. The device then performs a loop of monitoring about every second. In monitoring function, the device cycles sequentially through all measurements of temperatures and voltages and also performs the comparisons between readings and limits accordingly. The inputs are sampled in this order: Remote diode temperature, Local temperature, V_{DD}V_{IN}, 12V_{IN}, 5V_{IN}, 3.3V_{IN}, 2.5V_{IN} and V_{CCP}V_{IN}.

Measured values are stored in reading registers and results of limit comparison are reflected by the state of the flag bits in the status registers. Reading and status data can be read at any time. Limit values should be written into limit registers before starting conversion to avoid false conditions of the status.

Resetting (to 0) the START bit (bit 0) of the configuration register will stop the monitoring function and put the device into its standby mode thereby reducing power consumption.

Temperature measurement

The NE1619 contains an on-chip temperature sensor to measure the local or internal temperature and provides input pins (D– and D+) to measure the remote or external temperature with the use of a remote diode-type sensor. The remote sensor should be connected to the D– and D+ pins properly.

The method of temperature measurement is based on the change of the diode V_{BE} at two different operating current levels given by:

$$\Delta V_{BE} = (KT/q) * \ln(N)$$

where:

- K: Boltzmann's constant
- T: absolute temperature in °K
- q: charge on the electron
- N: ratio of the two currents
- LN: natural logarithm

The NE1619 provides two current sources of about 10 μA and 100 μA during the measurement of the remote diode V_{BE} and the sensed voltage between two pins D– and D+ is limited within 0.25 V and 0.95 V.

The external diode should be selected to meet this current and voltage requirements. The diode-connected PNP transistor provided on the Pentium series microprocessor is typically used, or the discrete diode-connected transistor 2N3904 is recommended.

For temperature measurement, local or remote, the ΔV_{BE} is converted into digital data by the on-chip sigma-delta A-to-D converter. The result is stored in the temperature reading register and is also compared with the limits stored in the temperature limit registers in order to set the temperature flag bits in the status register as described in Table 3.

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NAND-tree test

A NAND tree is provided in the NE1619 for Automated Test Equipment (ATE) board level connectivity testing. The device is placed into NAND tree test mode by powering up with Pin 9 (D-/NTEST_IN) held high. In this test mode Pin 16 (A0/RESET/NTEST_OUT) becomes the NAND-tree output and all input pins become NAND-tree inputs as illustrated in Figure 1.

To perform a NAND tree test all pins should be initially driven low. Then one-by-one toggle them high (and keep them high), starting with the input closest to the output, cycling toward the farthest, the NAND tree output will toggle with each input change.

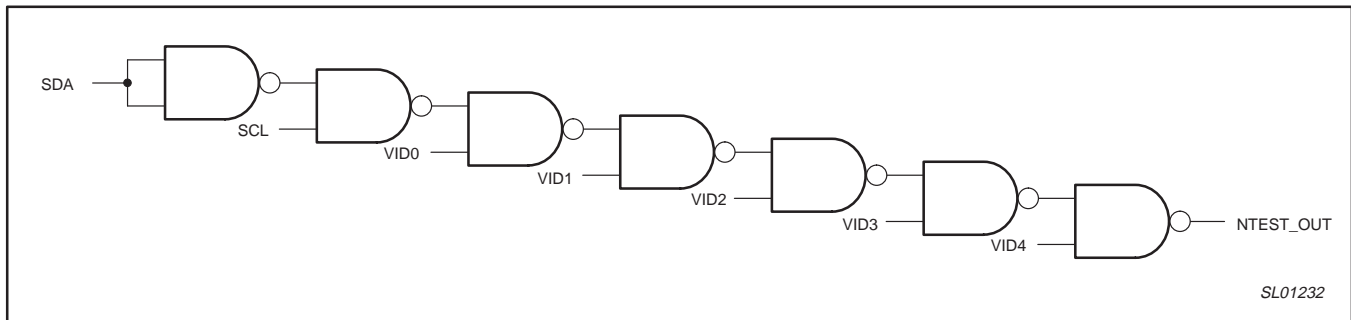


Figure 1. NAND-tree circuitry

Table 9. NAND-tree test vectors

VECTOR #	SDA	SCL	VID0	VID1	VID2	VID3	VID4	NTEST_OUT
1	L	L	L	L	L	L	L	H
2	L	L	L	L	L	L	H	L
3	L	L	L	L	L	H	H	H
4	L	L	L	L	H	H	H	L
5	L	L	L	H	H	H	H	H
6	L	L	H	H	H	H	H	L
7	L	H	H	H	H	H	H	H
8	H	H	H	H	H	H	H	L

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SMBus interface protocol

The NE1619 can communicate over a compatible 2-wire serial interface SMBus using the two device pins SCL and SDA. The device employs three standard SMBus protocols: Write Byte, Read Byte and Receive byte.

Data formats of those protocols are shown below with following notices:

- The SMBus controller initiates data transfer by establishing a start condition (S) and terminates data transfer by generating a stop condition (P).
- Data is sent over the serial bus in sequence of 9 clock pulses for each 8-bit data byte followed by 1-bit status of the device acknowledgement (A).

- The 7-bit slave address is replaced by the selected address of the device.
- The command byte is replaced by the selected command of the device register.
- The receive byte format is used for quickly transfer data from a reading register which was previously selected by a read.
- During the transition between start and stop conditions, data must be stable and valid when the SCL is high.

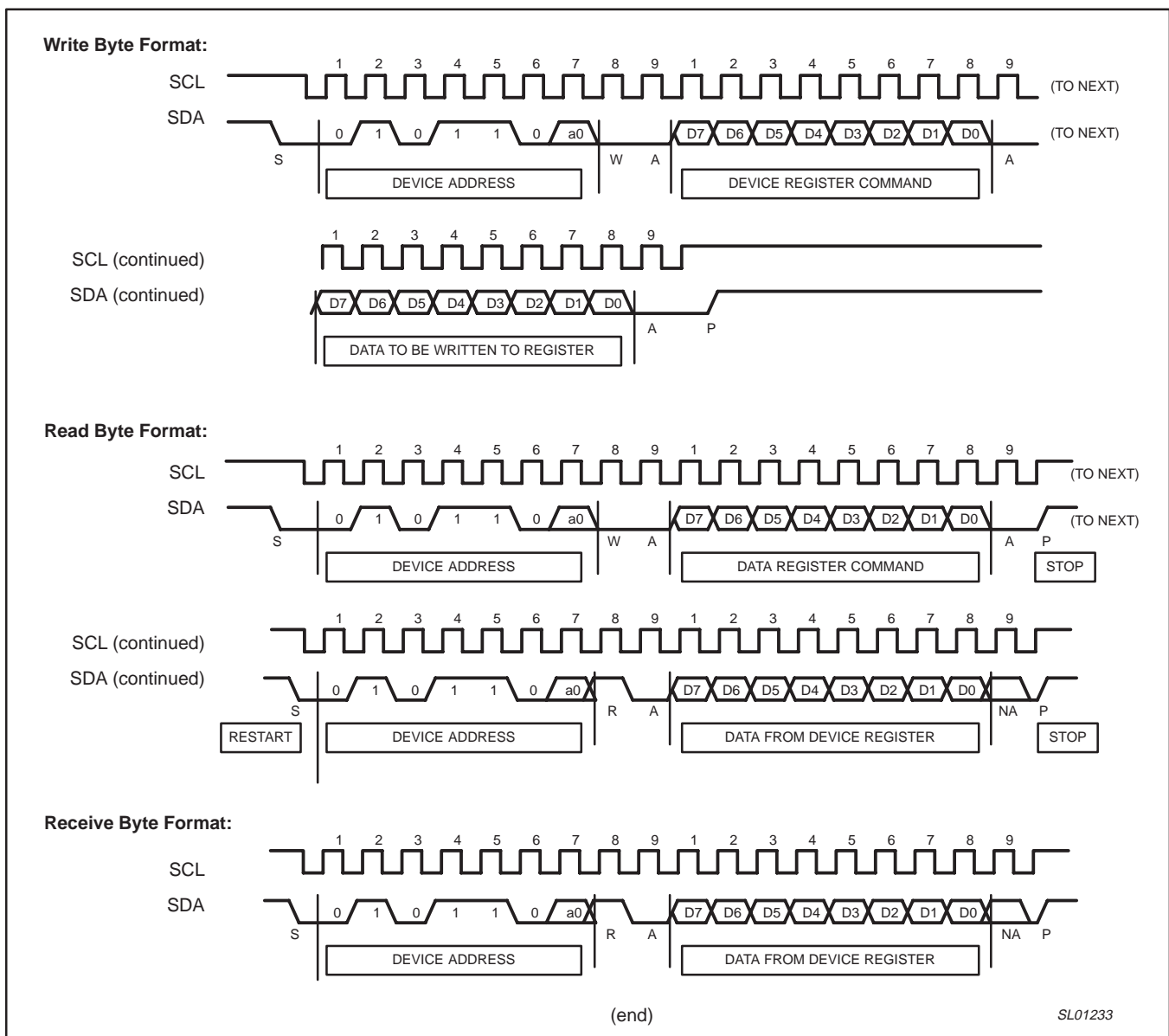


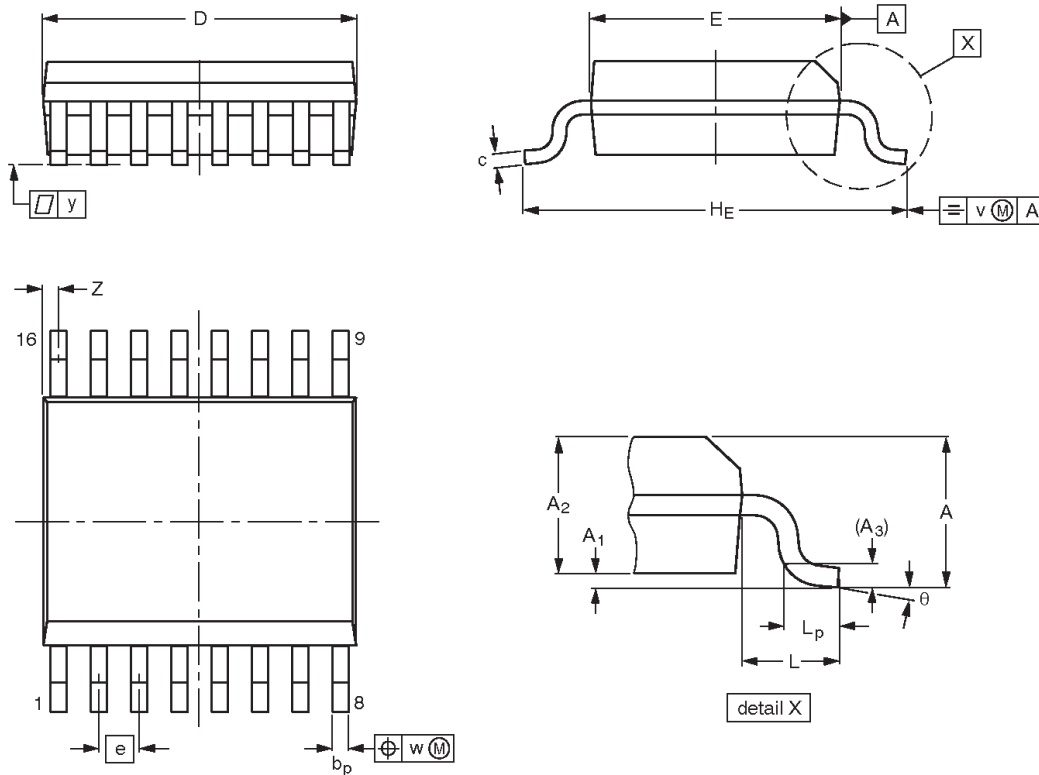
Figure 2. NE1619 SMBus interface protocols

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SSOP16: plastic shrink small outline package; 16 leads;
body width 3.9 mm; lead pitch 0.635 mm

SOT519-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	v	w	y	Z ⁽¹⁾	θ
mm	1.73	0.25 0.10	1.55 1.40	0.25	0.31 0.20	0.25 0.18	5.0 4.8	4.0 3.8	0.635	6.2 5.8	1.0	0.89 0.41	0.2	0.18	0.09	0.18 0.05	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT519-1						99-05-04

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NOTES

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Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definitions
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